Si5374

4-PLL Any-Frequency Precision Clock Multiplier/Jitter Attenuator

Features

- Highly-integrated, 4 PLL clock multiplier/jitter attenuator
- Four independent DSPLLs support any-frequency synthesis and jitter attenuation
- 8 inputs/8 outputs
- Each DSPLL can generate any frequency from 2 kHz to 808 MHz from a 2 kHz to 710 MHz input
- Ultra-low jitter clock outputs: 350 fs rms (12 kHz–20 MHz) and 410 fs rms (50 kHz–80 MHz) typical
- Meets ITU-T G.8251 and Telcordia GR-253-CORE OC-192 jitter specifications
- Supports all ITU G.709 and any custom FEC ratios (239/237, 255/238, 255/237, 255/236, 253/226)
- Integrated loop filter with programmable bandwidth
- Simultaneous free-run and synchronous operation
- Automatic/manual hitless input clock switching
- Selectable output clock signal format (LVPECL, LVDS, CML, CMOS)
- LOL and interrupt alarm outputs
- I^2C programmable
- Single 1.8 V ±5% or 2.5 V ±10% operation with high PSRR on-chip voltage regulator
- 10x10 mm PBGA

Ordering Information:

See page 63.

Applications

- High-density, any-port, any-protocol, any-frequency line cards
- ITU-T G.709 OTN custom FEC
- 10/40/100G
- OC-48/192, STM-16/64
- 1/2/4/8/10G Fibre Channel
- GbE/10 GbE Synchronous Ethernet
- Carrier Ethernet, multi-service switches and routers
- MSPP, ROADM, P-OTS, muxponders

Description

The Si5374 is a highly-integrated, 4-PLL, jitter-attenuating precision clock multiplier for applications requiring sub-1 ps jitter performance. Each of the DSPLL® clock multiplier engines accepts two input clocks ranging from 2 kHz to 710 MHz and generates two independent synchronous output clocks ranging from 2 kHz to 808 MHz. The device provides virtually any frequency translation combination across this operating range. For asynchronous, free-running clock generation applications, the Si5374's reference oscillator can be used as a clock source for any of the four DSPLLs. The Si5374 input clock frequency and clock multiplication ratio are programmable through an I^2C interface. The Si5374 is based on Silicon Laboratories' third-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly-integrated PLL solution that eliminates the need for external VCXO and loop filter components. Each DSPLL loop bandwidth is digitally-programmable, providing jitter performance optimization at the application level. The device operates from a single 1.8 or 2.5 V supply with on-chip voltage regulators with excellent PSRR. The Si5374 is ideal for providing clock multiplication and jitter attenuation in high-port-count optical line cards requiring independent timing domains.

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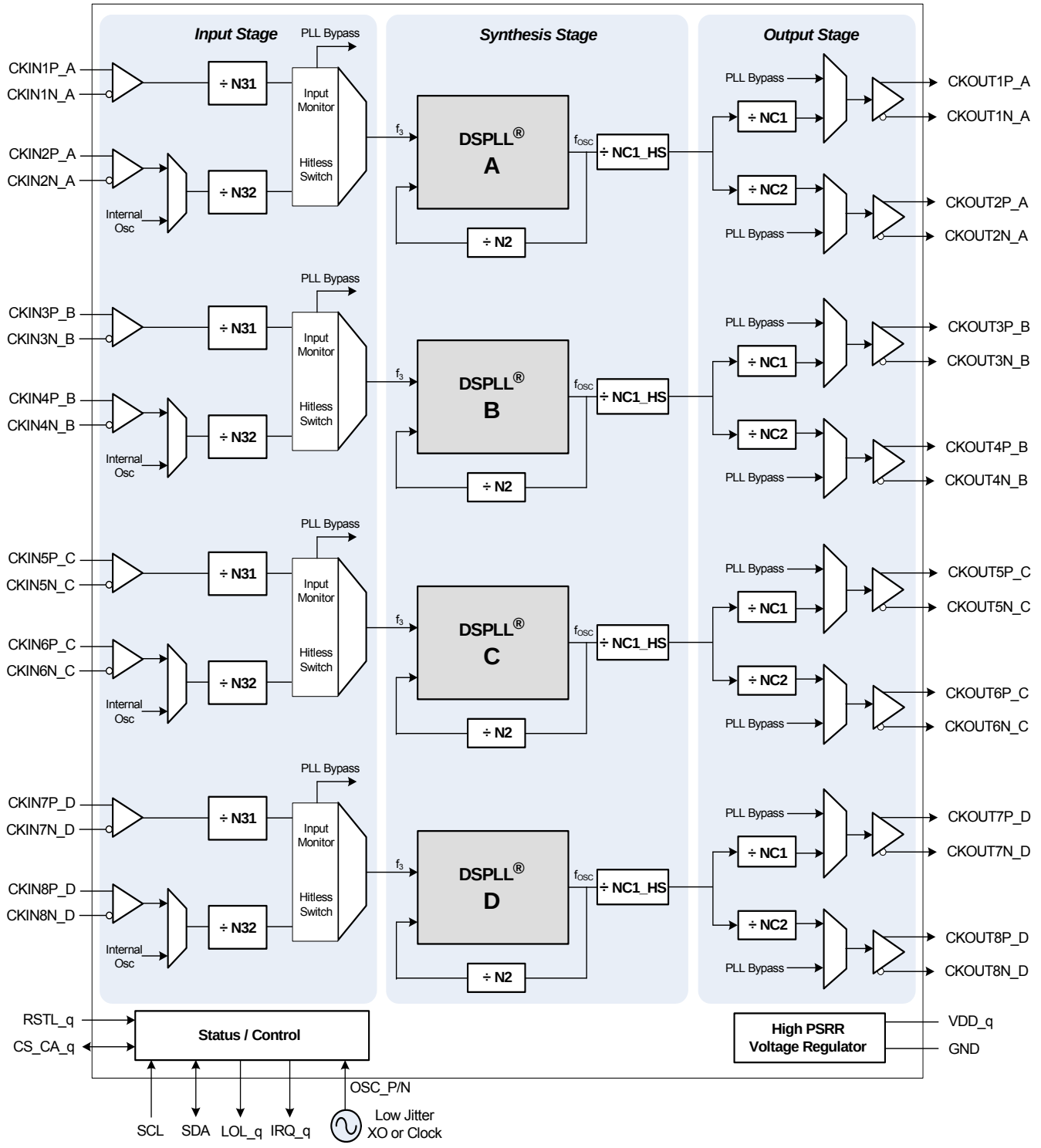
Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Supply Voltage during Normal Operation	V_{DD}	2.5 V Nominal	2.25	2.5	2.75	V
		1.8 V Nominal	1.71	1.8	1.89	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 ºC unless otherwise stated.						

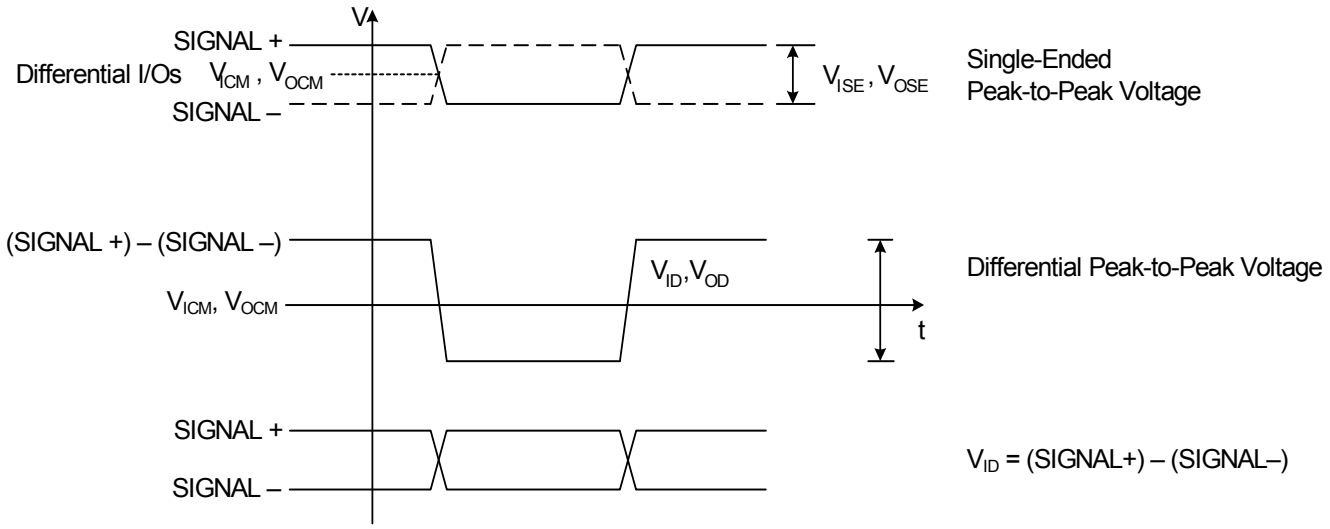


Figure 1. Differential Voltage Characteristics

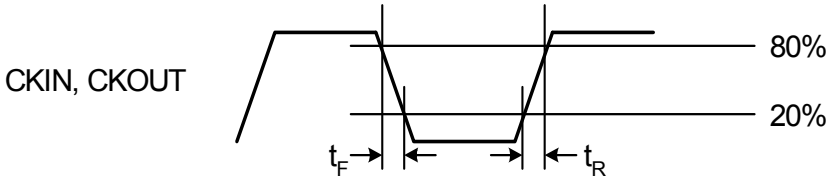


Figure 2. Rise/Fall Time Characteristics

Table 2. DC Characteristics
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1]	I_{DD}	LVPECL Format 622.08 MHz Out All CKOUTs Enabled	—	1000	1100	mA
		LVPECL Format 622.08 MHz Out 4 CKOUTs Enabled	—	870	970	mA
		CMOS Format 19.44 MHz Out All CKOUTs Enabled	—	820	940	mA
		CMOS Format 19.44 MHz Out 4 CKOUTs Enabled	—	780	880	mA
		Disable Mode	—	660	—	mA
CKINn Input Pins[2]						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ± 5%	0.9	—	1.4	V
		2.5 V ± 10%	1	—	1.7	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Single-Ended Input Voltage Swing (See Absolute Specs)	V_{ISE}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Differential Input Voltage Swing (See Absolute Specs)	V_{ID}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Output Clocks (CKOUTn)[3,4]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} –1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} = 2.5 V.
4. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single Ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD}–0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVPECL, LVDS	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V
Output Drive Current (CMOS driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally)	CKO_{IO}	ICMOS[1:0] = 11 V_{DD} = 1.8 V	—	7.5	—	mA
		ICMOS[1:0] = 10 V_{DD} = 1.8 V	—	5.5	—	mA
		ICMOS[1:0] = 01 V_{DD} = 1.8 V	—	3.5	—	mA
		ICMOS[1:0] = 00 V_{DD} = 1.8 V	—	1.75	—	mA
		ICMOS[1:0] = 11 V_{DD} = 2.5 V	—	20	—	mA
		ICMOS[1:0] = 10 V_{DD} = 2.5 V	—	15	—	mA
		ICMOS[1:0] = 01 V_{DD} = 2.5 V	—	10	—	mA
		ICMOS[1:0] = 00 V_{DD} = 2.5 V	—	5	—	mA

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} = 2.5 V.
4. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	IO = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
Output Voltage Low		IO = 2 mA V_{DD} = 2.25 V	—	—	0.4	V
Output Voltage High	V_{OH}	IO = –2 mA V_{DD} = 1.71 V	V_{DD} – 0.4	—	—	V
Output Voltage High		IO = –2 mA V_{DD} = 2.25 V	V_{DD} – 0.4	—	—	V

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} = 2.5 V.
4. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 3. AC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Reference Clock Input Pin OSC_P (OSC_N with cap to GND)[1]						
OSC_P to OSC_N Resistance	OSC_{RIN}	RATE_REG = 0101 or 0110, ac coupled	—	100	—	Ω
Input Voltage Swing	OSC_{VPP}	RATE_REG = 0101 or 0110, ac coupled	0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (OSC_P/OSC_N)[1]						
Input Voltage Swing	OSC_{VPP}	RATE_REG = 0101 or 0110, ac coupled	0.5	—	2.4	V_{PP}
CKINn Input Pins						
Input Frequency	CKN_F		0.002	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high-frequency clocks)	40	—	60	%
			2	—	—	ns
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins						
Output Frequency (Output not configured for CMOS or Disabled)	CKO_F		0.002	—	808	MHz
Maximum Output Frequency in CMOS Format	CKO_F		—	—	212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO_{TRF}	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 1.71 C_{LOAD} = 5 pF	—	—	8	ns
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 2.25 C_{LOAD} = 5 pF	—	—	2	ns

Notes:
1. A crystal may not be used in place of an oscillator.
2. Input to output skew after an ICAL is not controlled and can be any value.

Table 3. AC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO_{DC}	100 Ω Load Line-to-Line Measured at 50% Point (differential)	—	—	±40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMN}		1	—	—	µs
Reset to Microprocessor Access Ready	t_{READY}		—	—	10	ms
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20pf See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKINn ↑ to ↓ Internal detection of LOSn N3 ≠ 1	—	—	4.5 x N3	T_{CKIN}
Time to Clear LOL after LOS Cleared	t_{CLRLOL}	↓LOS to ↓LOL Fold = Fnew Stable OSC_P, OSC_N reference	—	10	—	ms

Notes:
1. A crystal may not be used in place of an oscillator.
2. Input to output skew after an ICAL is not controlled and can be any value.

Table 3. AC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Device Skew[2]						
Output Clock Skew	t_{SKEW}	↑ of CKOUTn to ↑ of CKOUT_m, CKOUTn and CKOUT_m at same frequency and signal format PHASEOFFSET = 0 CKOUT_ALWAYS_ON = 1 SQ_ICAL = 1	—	—	100	ps
Phase Change due to Temperature Variation	t_{TEMP}	Max phase changes from –40 to +85 °C	—	300	500	ps

Notes:
1. A crystal may not be used in place of an oscillator.
2. Input to output skew after an ICAL is not controlled and can be any value.

Table 4. Microprocessor Control
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I^2C Bus Lines (SDA, SCL)						
Input Voltage Low	VIL_{I2C}		—	—	0.25 x V_{DD}	V
Input Voltage High	VIH_{I2C}		0.7 x V_{DD}	—	V_{DD}	V
Hysteresis of Schmitt Trigger Inputs	$VHYS_{I2C}$	V_{DD} = 1.8 V	0.1 x V_{DD}	—	—	V
		V_{DD} = 2.5	0.05 x V_{DD}	—	—	V
Output Voltage Low	VOL_{I2C}	V_{DD} = 1.8 V IO = 3 mA	—	—	0.2 x V_{DD}	V
		V_{DD} = 2.5 IO = 3 mA	—	—	0.4	V

Table 5. Performance Specifications

V_{DD} = 1.8 V ±5% or 2.5 V ±10%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Performance[1]						
Lock Time[2] Si5374B-A-xL[3]	t_{LOCKMP}	Start of ICAL to ↓ of LOL, FASTLOCK enabled	—	1	1.5	s
Si5374C-A-xL			—	0.8	1.0	
Settle Time[2] Si5374B-A-xL	t_{SETTLE}	Start of ICAL to F_{OUT} within 5 ppm of final value	—	1.2	1.5	s
Si5374C-A-xL			—	4.2	5.0	
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise fout = 622.08 MHz	CKO_{PN}	1 kHz Offset	—	–106	—	dBc/Hz
		10 kHz Offset	—	–114	—	dBc/Hz
		100 kHz Offset	—	–116	—	dBc/Hz
		1 MHz Offset	—	–132	—	dBc/Hz
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	–70	—	dBc
Jitter Generation	J_{GEN}	f_{IN} = f_{OUT} = 622.08 MHz, BW = 120 Hz LVPECL output 12 kHz–20 MHz	—	350	410	fs rms
		50 kHz–80 MHz	—	410	—	fs rms

Notes:

1. fin = fout = 622.08 MHz; BW = 7 Hz; LVDS, OSC = .121.109 MHz.
2. Lock and settle time performance is dependent on the frequency plan and the OSC_P/OSC_N reference frequency and LOCKT setting (see application note, "AN803: Lock and Settling Time Considerations for the Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs". Visit the Silicon Labs Technical Support web page at: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.
3. LOCKT = 3.3 ms.

Table 6. Thermal Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Junction Temperature			—	125	—	°C
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air Air Flow 1 m/s Air Flow 2 m/s Air Flow 3 m/s	— — — —	16 14 13 12	— — — —	°C/W
Thermal Resistance Junction to Case	φ_{JC}	Still Air	—	3.4	—	°C/W

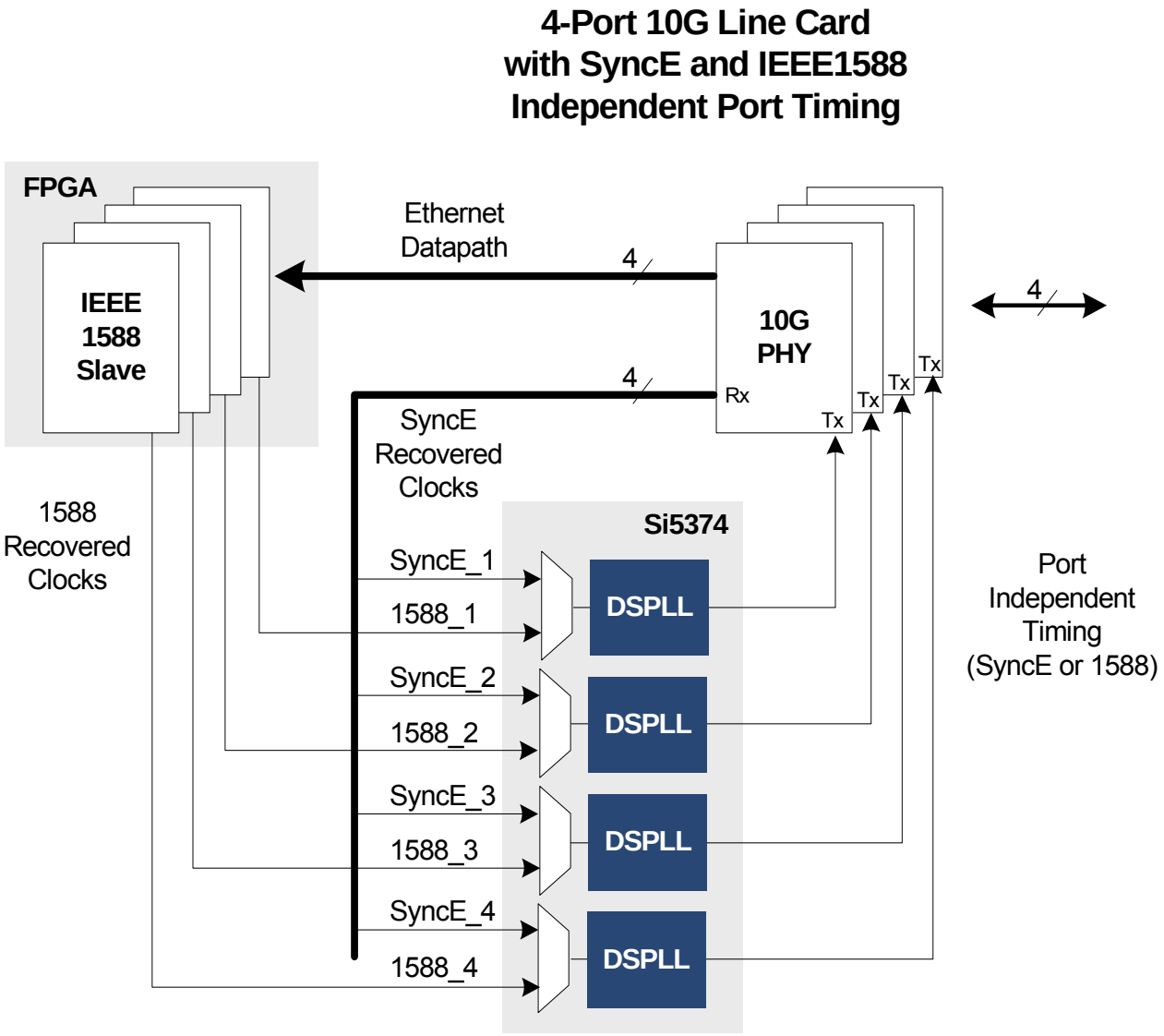
Notes:
1. In most circumstances the Si5374 does not require special thermal management. A system level thermal analysis is strongly recommend. Contact Silicon Labs applications for further details if required.
2. Thermal characteristic for the 80-pin Si5374 on an 8-layer PCB.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 2.8	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
CLKINnP/N_q	CKN_{VIN}	0 to V_{DD}	V
OSC_P, OSC_N Voltage Limits	OSC_{VIN}	0 to 1.2	V
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
ESD HBM Tolerance (100 pF, 1.5 k); All pins except CKINnP/N-q		2	kV
ESD MM Tolerance; All pins except CKINnP/N_q		200	V
ESD HBM Tolerance (100 pF, 1.5 k); CKINnP/N_q		700	V
ESD MM Tolerance; CKINnP/N_q		125	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

2. Typical Application Schematic



3. Typical Phase Noise Plot

- 19.44 MHz input
- 698.8123 MHz OTU4 output
- 334 fs RMS jitter (12 kHz to 20 MHz)

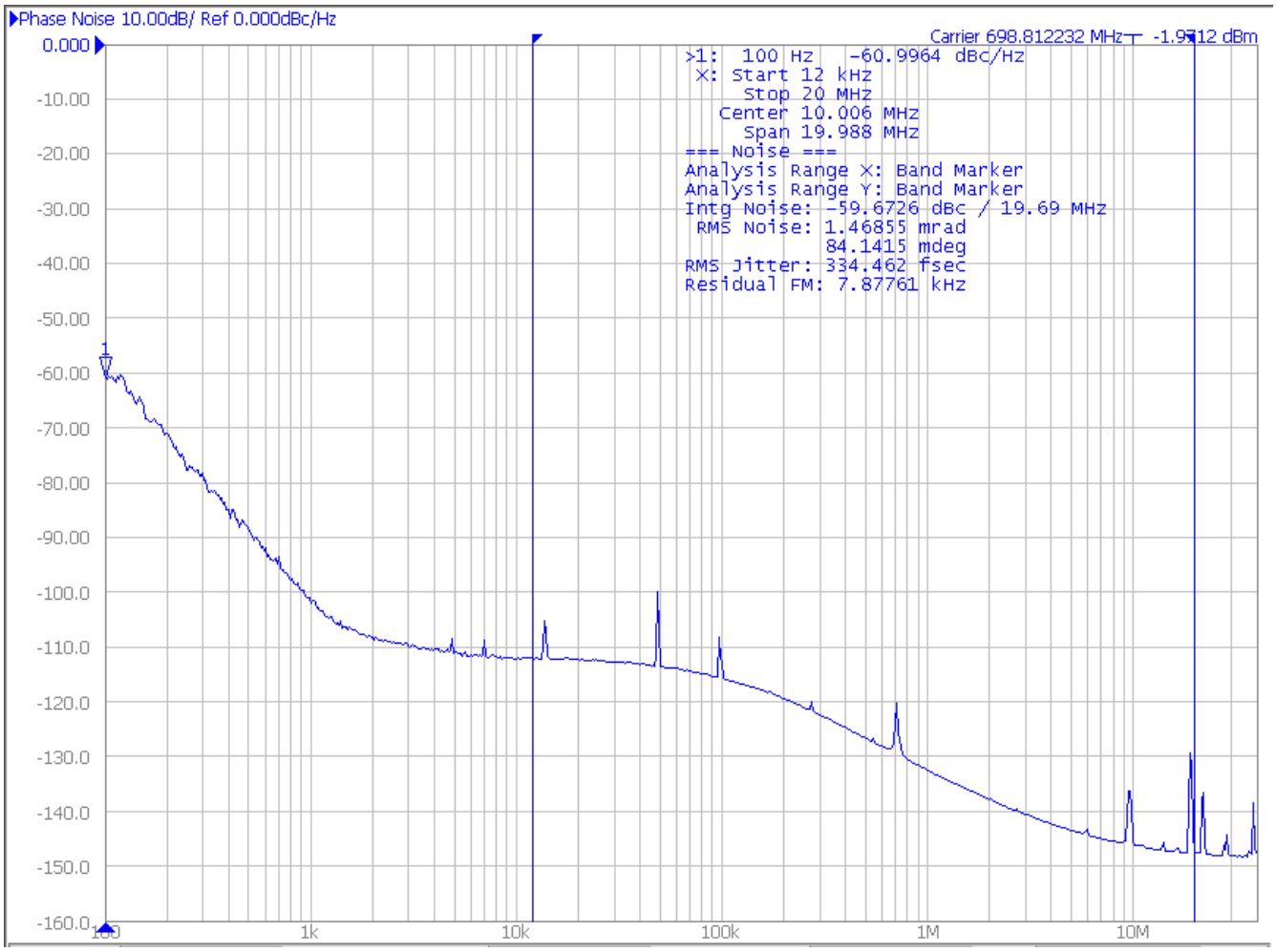


Figure 3. Typical Phase Noise Plot

4. Functional Description

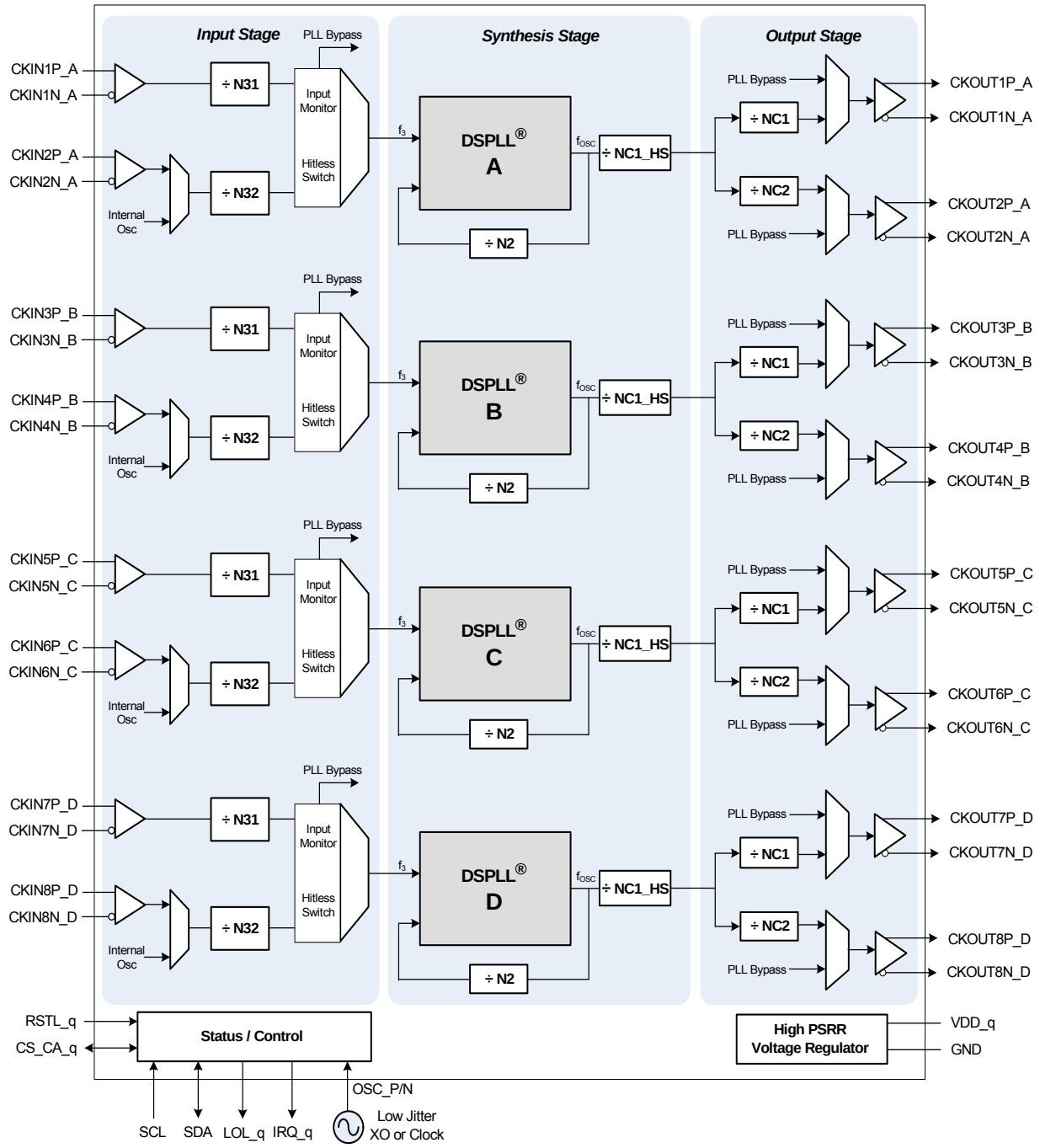


Figure 4. Functional Block Diagram

The Si5374 is a highly integrated jitter-attenuating clock multiplier that integrates four fully independent DSPLLs and provides ultra-low jitter generation with less than 410 fs RMS. Configuration and control of the Si5374 is mainly handled through the I^2C interface. The device accepts clock inputs ranging from 2 kHz to 710 MHz and generates independent, synchronous clock outputs ranging from 2 kHz to 808 MHz for each DSPLL. Virtually any frequency translation (M/N) combination across its operating range is supported. The Si5374 supports a digitally programmable loop bandwidth that can range from 4 to 525 Hz requiring no external loop filter components. An external single-ended or differential reference clock or XO is required for the device to enable ultra-low jitter generation and jitter attenuation.

The device monitors each input clock for loss-of-signal (LOS) and provides a LOS alarm when missing pulses on any of the input clocks are detected. The device monitors the lock status of each DSPLL and provides a Loss-of-Lock (LOL) alarm when the DSPLL is unlocked. The lock detect algorithm continuously monitors the phase of the selected input clock in relation to the phase of the feedback clock. See application note, "AN803: Lock and Settling Time Considerations for the Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs."

The Si5374 provides a holdover capability that allows the device to continue generation of a stable output clock when the input reference is lost. The reference oscillator can be internally routed into CKIN2_q, so free-running clock generation is supported for each DSPLL offering simultaneous synchronous and asynchronous operation.

The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, CML, and CMOS loads. If the CMOS signal format is selected, each differential output buffer generates two in-phase CMOS clocks at the same frequency. For system-level debugging, a DSPLL bypass mode drives the clock output directly from the selected input clock, bypassing the internal DSPLL.

Silicon Laboratories offers a PC-based software utility, Si537xDSPLL*sim* that can be used to determine valid frequency plans and loop bandwidth settings to simplify device setup. Si537xDSPLL*sim* provides the optimum input, output, and feedback divider values for a given input frequency and clock multiplication ratio that minimizes phase noise. This utility can be downloaded from http://www.silabs.com/timing. For further assistance, refer to the Si53xx Any-Frequency Precision Clocks Family Reference Manual.

5. Si5374 Application Examples and Suggestions

5.1. Schematic and PCB Layout

For a typical application schematic and PCB layout, see the Si537x-EVB Evaluation Board User's Guide, which can be downloaded from www.silabs.com/timing.

In order to preserve the ultra low jitter of the Si5374 in applications where the four different DSPLL's are each operating at different frequency, special care and attention must be paid to the PCB layout. The following is a list of rules that should be observed:

1. The four Vdd supplies should be isolated from one another with four ferrite beads. They should be separately bypassed with capacitors that are located very close to the Si5374 device.
2. Use a solid and undisturbed ground plane for the Si5374 and all of the clock input and output return paths.
3. For applications that wish to logically connect the four RESET signals, do not tie them together underneath the BGA package. Instead connect them outside of the BGA footprint.
4. As much as is possible, do not route clock input and output signals underneath the BGA package. The clock output signals should go directly outwards from the BGA footprint.
5. Avoid placing the OSC_P and OSC_N signals on the same layer as the clock outputs. Add grounded guard traces surrounding the OSC_P and OSC_N signals.
6. Where possible, place the CKOUT and CKIN signals on separate PCB layers with a ground layer between them. The use of ground guard traces between all clock inputs and outputs is recommended.

For more information, see the Si537x-EVB Evaluation Board User's Guide and Appendix I of the Si53xx Reference Manual, Rev 0.5 or higher.

5.2. Thermal Considerations

The Si5374 dissipates a significant amount of heat and it is important to take this into consideration when designing the Si5374 operating environment. Among other issues, high die temperatures can result in increased jitter and decreased long term reliability. It is therefore recommended that one or more of the following occur:

1. Use a heat sink - A heat sink example is Aavid part number 375324B00035G.
2. Use a Vdd voltage of 1.8 V.
3. Limit the ambient temperature to significantly less that 85 °C.
4. Implement very good air flow.

5.3. SCL Leakage

When selecting pull up resistors for the two I^2C signals, note that there is an internal pull down resistor of 18 kΩ from the SCL pin to ground. This comment does not apply to the SDA pin.

5.4. RSTL_x Pins

It is recommended that the four RSTL_x pins (RSTL_A, RSTL_B, RSTL_C and RSTL_D) be logically connected together such that all four DSPLLs are either in or out of reset mode. When a DSPLL is in reset mode, its VCO will not be locked to any signal and may drift across its operating range. If a drifting VCO has a frequency similar to that of an operating VCO, there could be some crosstalk between the two VCOs. To avoid this from occurring during device initialization, DSPLLsim loads each DSPLL with default Free Run frequency plans with VCO values apart from one another. If the four RSTL_x pins are directly connected to one another, the connections should not be made directly underneath the BGA package. Instead, the connections should be made outside the package footprint.

5.5. Reference Oscillator Selection

Care should be taken during the selection of the external oscillator that is connected to the OSC_P and OSC_N pins. There is no jitter attenuation from the OSC reference inputs to the output; so, to achieve low output jitter, a low-jitter reference OSC must be used. Also, the output drift during holdover will be the same as the drift of the OSC reference. For example, a Stratum 3 application will require an OSC reference source that has Stratum 3 stability (though Stratum 3 accuracy is not required).

The OSC frequency can be any value from 109 to 125.5 MHz. See the RATE_REG (reg 2) description. Alternately, for applications with less demanding jitter requirements, the OSC frequency can be in the range from 37 to 41 MHz. For applications that use Free Run mode, the freedom to use any OSC frequency within these bands can be used to select an OSC frequency that has an integer relationship to the desired output frequency, which will make it easier to find a high-performance frequency plan.

If Free Run is not being used, an OSC frequency that is not integer-related to the output frequency is preferred. A recommended choice for an external oscillator is the Silicon Labs 530EB121M109DG, which is a 2.5 V, LVPECL device with a temperature stability of 20 ppm. It was used to take the typical phase noise plot on page 14. For more details and a more complete discussion of these topics, see the Si53xx Reference Manual.

The very low loop BW of the Si5374 means that it can be susceptible to OSC_P/OSC_N reference sources

that have high wander. Experience has shown that in spite of having low jitter, some MEMs oscillators have high wander, and these devices should be avoided. Silicon Labs does not recommend using MEMS based oscillators as the Si5374 frequency reference. Contact Silicon Labs for details.

5.6. Alarms

To assist in the programming of the IRQ_n pins, refer to the below diagram of the Si5374 alarm structure.

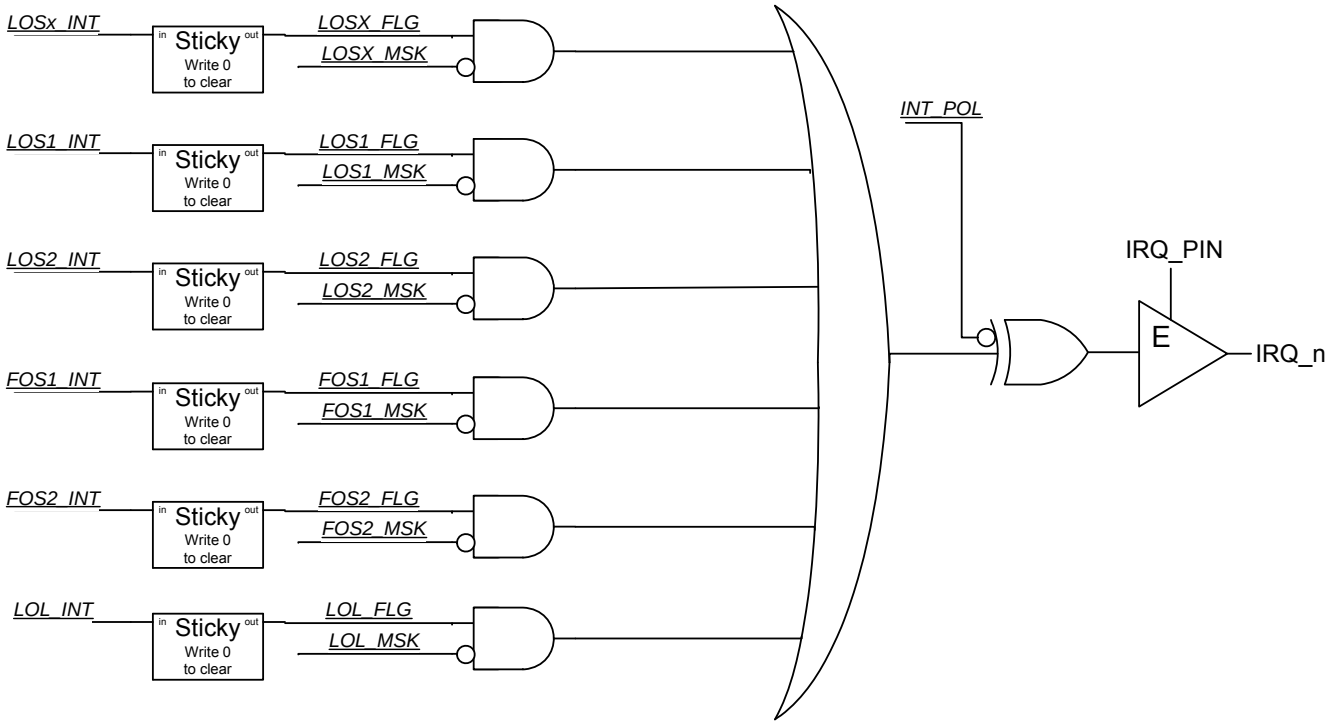


Figure 5. Si5374 Alarm Structure

5.7. OSC_P and OSC_N Connection

Figures 6, 7, and 8 show examples of connecting various OSC reference sources to the OSC_P and OSC_N pins. A crystal may not be used in place of an external oscillator.

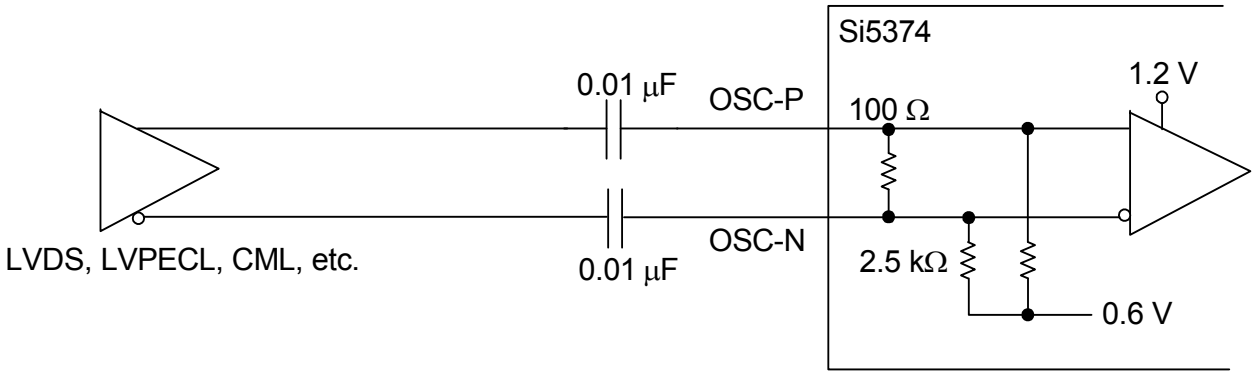


Figure 6. Differential OSC Reference Input Example for Si5374

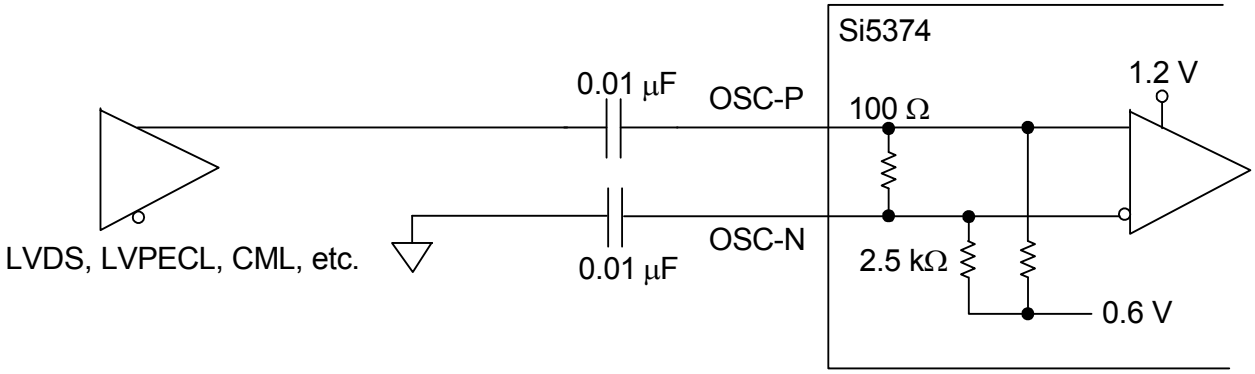


Figure 7. Single-Ended OSC Reference Input Example for Si5374

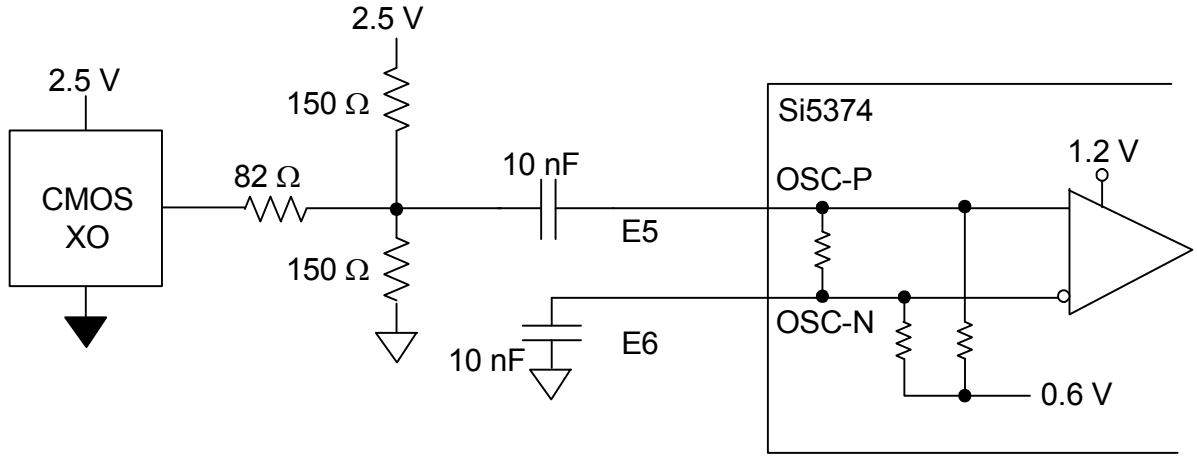


Figure 8. Single-Ended, 2.5 V, CMOS XO Connection

6. Register Map

The Si5374 has four identical register maps for each DSPLL. Each DSPLL has a unique I^2C address enabling independent control and device configuration. The I^2C address is 11010 [A1] [A0] for the entire device. Each corresponding DSPLL [A1] [A0] address is fixed as below.

	[A1]	[A0]
DSPLLA:	0	0
DSPLLB:	0	1
DSPLLC:	1	0
DSPLLD:	1	1

Note: The Si5374 register map is similar, but not identical, to the Si5324 device.

All register bits that are not defined in this map should always be written with the specific reset values. Writing to these bits with values other than the specified reset values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

Table 8. Si5374 Registers

Reg.	D7	D6	D5	D4	D3	D2	D1	D0
0		FREE_RUN	CKOUT_ ALWAYS_ON				BYPASS_REG	
1					CK_PRIOR2[1:0]		CK_PRIOR1[1:0]	
2	BWSEL_REG[3:0]				RATE_REG [3:0]			
3	CKSEL_REG[1:0]		DHOLD	SQ_ICAL				
4	AUTOSEL_REG[1:0]			HIST_DEL[4:0]				
5	ICMOS[1:0]							
6			SFOUT2_REG[2:0}			SFOUT1_REG[2:0]		
7						FOSREFSEL[2:0]		
8	HLOG_2[1:0]		HLOG_1[1:0]					
9	HIST_AVG[4:0]							
10					DSBL2_ REG	DSBL1_ REG		
11							PD_CK2	PD_CK1
19	FOS_EN	FOS_THR[1:0]		VALTIME[1:0]		LOCKT[2:0]		
20					Write 0	Write 0	LOL_PIN	IRQ_PIN
21	Write 0	Write 0					CK1_ACT-V_PIN	CKSEL_PIN
22					CK_ACTV_ POL		LOL_POL	INT_POL
23						LOS2_MSK	LOS1_MSK	LOSX_MSK
24						FOS2_MSK	FOS1_MSK	LOL_MSK
25	N1_HS[2:0]							
31					NC1_LS[19:16]			
32	NC1_LS[15:8]							

Table 8. Si5374 Registers (Continued)

Reg.	D7	D6	D5	D4	D3	D2	D1	D0
33	NC1_LS[7:0]							
34					NC2_LS[19:16]			
35	NC2_LS[15:8]							
36	NC2_LS[7:0]							
40	N2_HS[2:0]				N2_LS[19:16]			
41	N2_LS[15:8]							
42	N2_LS[7:0]							
43						N31[18:16]		
44	N31[15:8]							
45	N31[7:0]							
46						N32[18:16]		
47	N32[15:8]							
48	N32[7:0]							
55			CLKIN2RATE[2:0]			CLKIN1RATE[2:0]		
128							CK2_ACT-V_REG	CK1_ACT-V_REG
129						LOS2_INT	LOS1_INT	LOSX_INT
130		DIGHOLD VALID				FOS2_INT	FOS1_INT	LOL_INT
131						LOS2_FLG	LOS1_FLG	LOSX_FLG
132					FOS2_FLG	FOS1_FLG	LOL_FLG	
134	PARTNUM_RO[11:4]							
135	PARTNUM_RO[3:0]				REVID_RO[3:0]			
136	RST_REG	ICAL						
137								FASTLOCK
138							LOS2_EN [1:1]	LOS1_EN [1:1]
139			LOS2_EN[0:0]	LOS1_EN[0:0]			FOS2_EN	FOS1_EN
142	INDEPENDENTSKEW1[7:0]							
143	INDEPENDENTSKEW2[7:0]							

7. Register Descriptions

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FREE_RUN	CKOUT_ALWAYS_ON				BYPASS_REG	
Type	R	R/W	R/W	R	R	R	R/W	R

Reset value = 0001 0100

Bit	Name	Function
7	Reserved	**Reserved.**
6	FREE_RUN	**Free Run.** Internal to the device, route XA/XB to CKIN2. This allows the DSPLL to lock to its XA-XB reference to support free-running clock generation. 0: Disable 1: Enable
5	CKOUT_ALWAYS_ON	**CKOUT Always On.** This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 9 on page 56. 0: Squelch output until device is calibrated (ICAL). 1: Provide an output. **Notes:** **1.** The frequency may be significantly off until the device is calibrated. **2.** Must be set to 1 to control output to output skew.
4:2	Reserved	**Reserved.**
1	BYPASS_REG	**Bypass Register.** This bit enables or disables PLL bypass mode. Use only when the device is in digital hold or before the first ICAL. Bypass mode does not support CMOS clock outputs. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL.
0	Reserved	**Reserved.**

Register 1.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CK_PRIOR2 [1:0]		CK_PRIOR1 [1:0]	
Type	R				R/W		R/W	

Reset value = 1110 0100

Bit	Name	Function
7:4	Reserved	
3:2	CK_PRIOR2 [1:0]	**2nd Priority Input Clock.** Selects which of the input clocks will be 2nd priority in the autoselection state machine. 00: CKIN1 is 2nd priority. 01: CKIN2 is 2nd priority. 10: Reserved 11: Reserved
1:0	CK_PRIOR1 [1:0]	**1st Priority Input Clock.** Selects which of the input clocks will be 1st priority in the autoselection state machine. 00: CKIN1 is 1st priority. 01: CKIN2 is 1st priority. 10: Reserved 11: Reserved

Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BWSEL_REG [3:0]				RATE_REG[3:0]			
Type	R/W				R/W			

Reset value = 0100 0010

Bit	Name	Function
7:4	BWSEL_REG [3:0]	**BWSEL_REG.** Selects nominal f3dB bandwidth for PLL. See Si53xDSPLLsim for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.
3:0	RATE_REG [3:0]	**RATE Setting for Oscillator.** An external oscillator or other clock source must be used. It is not possible to use just a crystal. Setting / Minimum / Recommended / Maximum / Units 0101 / 37 / 40 / 41 / MHz 0110 / 109 / 121.109 / 125.5 / MHz Others: Reserved

Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CKSEL_REG[1:0]		DHOLD	SQ_ICAL				
Type	R/W		R/W	R/W	R	R	R	R

Reset value = 0000 0101

Bit	Name	Function
7:6	CKSEL_REG [1:0]	**CKSEL_REG.** If the device is operating in register-based manual clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1 and AUTOSEL_REG = 00, the CS_CA input pin continues to control clock selection and CKSEL_REG is of no consequence. 00: CKIN_1 selected. 01: CKIN_2 selected. 10: Reserved 11: Reserved
5	DHOLD	**DHOLD.** Forces the device into digital hold. This bit overrides all other manual and automatic clock selection controls. 0: Normal operation. 1: Force digital hold mode. Overrides all other settings and ignores the quality of the input clocks.
4	SQ_ICAL	**SQ_ICAL.** This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 9 on page 56. 0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.
3:0	Reserved	

Register 4.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTOSEL_REG [1:0]			HIST_DEL [4:0]				
Type	R/W		R	R/W				

Reset value = 0001 0010

Bit	Name	Function
7:6	AUTOSEL_REG [1:0]	**AUTOSEL_REG [1:0].** Selects input clock selection control method. 00: Manual (either register or pin controlled, see CKSEL_PIN) 01: Automatic non-revertive 10: Automatic revertive 11: Reserved
5	Reserved	
4:0	HIST_DEL [4:0]	**HIST_DEL [4:0].** Selects amount of delay to be used in generating the history information used for Digital Hold.

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ICMOS [1:0]							
Type	R/W		R	R	R	R	R	R

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	**ICMOS [1:0].** When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 2.5 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT-. 00: 5 mA/1.75 mA 01: 10 mA/3.5 mA 10: 15 mA/5.5 mA 11: 20 mA/7.5 mA
5:0	Reserved	

Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			SFOUT2_REG [2:0]			SFOUT1_REG [2:0]		
Type	R	R	R/W			R/W		

Reset value = 0010 1101

Bit	Name	Function
7:6	Reserved	
5:3	SFOUT2_ REG [2:0]	**SFOUT2_REG [2:0].** Controls output signal format and disable for CKOUT2 output buffer. 000: Reserved 001: Disable CKOUT2 010: CMOS (Bypass mode not supported) 011: Low swing LVDS 100: Reserved 101: LVPECL (not available when V_{DD} = 1.8 V) 110: CML 111: LVDS
2:0	SFOUT1_ REG [2:0]	**SFOUT1_REG [2:0].** Controls output signal format and disable for CKOUT1 output buffer. 000: Reserved 001: Disable CKOUT1 010: CMOS (Bypass mode not supported) 011: Low swing LVDS 100: Reserved 101: LVPECL (not available when V_{DD} = 1.8 V) 110: CML 111: LVDS

Register 7.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						FOSREFSEL [2:0]		
Type	R	R	R	R	R	R/W		

Reset value = 0010 1010

Bit	Name	Function
7:3	Reserved	
2:0	FOSREFSEL [2:0]	**FOSREFSEL [2:0].** Selects which input clock is used as the reference frequency for Frequency offset (FOS) monitoring. 000: OSC (External reference) 001: CKIN1 010: CKIN2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Register 8.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HLOG_2[1:0]		HLOG_1[1:0]					
Type	R/W		R/W		R	R	R	R

Reset value = 0000 0000

Bit	Name	Function
7:6	HLOG_2 [1:0]	**HLOG_2 [1:0].** 00: Normal operation 01: Holds CKOUT2 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10:Holds CKOUT2 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
5:4	HLOG_1 [1:0]	**HLOG_1 [1:0].** 00: Normal operation 01: Holds CKOUT1 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT1 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
3:0	Reserved	

Register 9.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HIST_AVG [4:0]							
Type	R/W					R	R	R

Reset value = 1100 0000

Bit	Name	Function
7:3	HIST_AVG [4:0]	**HIST_AVG [4:0].** Selects amount of averaging time to be used in generating frequency history information for Digital Hold.
2:0	Reserved	

Register 10.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					DSBL2_REG	DSBL1_REG		
Type	R	R	R	R	R/W	R/W	R	R

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3	DSBL2_REG	**DSBL2_REG.** This bit controls the powerdown of the CKOUT2 output buffer. If disable mode is selected, the NC2 output divider is also powered down. 0: CKOUT2 enabled 1: CKOUT2 disabled
2	DSBL1_REG	**DSBL1_REG.** This bit controls the powerdown of the CKOUT1 output buffer. If disable mode is selected, the NC1 output divider is also powered down. 0: CKOUT1 enabled 1: CKOUT1 disabled
1:0	Reserved	

Register 11.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							PD_CK2	PD_CK1
Type	R	R	R	R	R	R	R/W	R/W

Reset value = 0100 0000

Bit	Name	Function
7:2	Reserved	
1	PD_CK2	**PD_CK2.** This bit controls the powerdown of the CKIN2 input buffer. 0: CKIN2 enabled 1: CKIN2 disabled
0	PD_CK1	**PD_CK1.** This bit controls the powerdown of the CKIN1 input buffer. 0: CKIN1 enabled 1: CKIN1 disabled

Register 19.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FOS_EN	FOS_THR [1:0]		VALTIME [1:0]		LOCKT [2:0]		
Type	R/W	R/W		R/W		R/W		

Reset value = 0010 1100

Bit	Name	Function
7:5	FOS_EN	**FOS_EN.** Frequency Offset Enable globally disables FOS. See the individual FOS enables (FOS-X_EN, register 139). 0: FOS disable 1: FOS enabled by FOSx_EN
6:5	FOS_THR [1:0]	**FOS_THR [1:0].** Frequency Offset at which FOS is declared: 00: ± 11 to 12 ppm (Stratum 3/3E compliant, with a Stratum 3/3E used for REFCLK. 01: ± 48 to 49 ppm SONET Minimum Clock (SMC) with SMC used for REFCLK. 10: ± 30 ppm (SONET Minimum Clock (SMC), with a Stratum 3/3E used for REFCLK. 11: ± 200 ppm
4:3	VALTIME [1:0]	**VALTIME [1:0].** Sets amount of time for input clock to be valid before the associated alarm is removed. 00: 2 ms 01: 100 ms 10: 200 ms 11: 13 seconds
2:0	LOCKT [2:0]	**LOCKT [2:0].** Sets retrigger interval for one shot monitoring phase detector output. One shot is triggered by phase slip in DSPLL. To minimize lock time during an ICAL, a LOCKT value of 001 is recommended. Refer to the Family Reference Manual and application note, "AN803: Lock and Settling Time Considerations for the Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs", for more details. 000: 106 ms 001: 53 ms 010: 26.5 ms 011: 13.3 ms 100: 6.6 ms 101: 3.3 ms 110: 1.66 ms 111: 0.833 ms

Register 20.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					Write 0	Write 0	LOL_PIN	IRQ_PIN
Type	R	R	R	R	W	W	R/W	R/W

Reset value = 0011 1110

Bit	Name	Function
7:4	Reserved	
3:2	Write 0	**Write to zero.**
1	LOL_PIN	**LOL_PIN.** The LOL_INT status bit can be reflected on the LOL output pin. 0: LOL output pin tristated 1: LOL_INT status reflected to output pin
0	IRQ_PIN	**IRQ_PIN.** Reflects interrupt status on the IRQ output pin. 0: Output is disabled. 1: Output is enabled.

Register 21.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Write 0	Write 0					CK1_ACTV_PIN	CKSEL_ PIN
Type	W	W	R	R	R	R	R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7:6	Write 0	**Write zero.**
5:2	Reserved	
1	CK1_ACTV_PIN	**CK1_ACTV_PIN.** The CK1_ACTV_REG status bit can be reflected to the CS_CA output pin using the CK1_ACTV_PIN enable function. CK1_ACTV_PIN is of consequence only when pin controlled clock selection is being used. 0: CS_CA output pin tristated. 1: Clock Active status reflected to output pin.
0	CKSEL_PIN	**CKSEL_PIN.** If manual clock selection is used, clock selection can be controlled via the CKSEL_REG[1:0] register bits or the CS_CA input pin. This bit is only active when AUTOSEL_REG = Manual. 0: CS_CA pin ignored. CKSEL_REG[1:0] register bits control clock selection. 1: CS_CA input pin controls clock selection.

Register 22.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CK_ACTV_POL		LOL_POL	INT_POL
Type	R	R	R	R	R/W	R	R/W	R/W

Reset value = 1101 1111

Bit	Name	Function
7:4	Reserved	
3	CK_ACTV_ POL	**CK_ACTV_POL.** Sets the active polarity for the CS_CA signals when reflected on an output pin. 0: Active low 1: Active high
2	Reserved	
1	LOL_POL	**LOL_POL.** Sets the active polarity for the LOL status when reflected on an output pin. 0: Active low 1: Active high
0	INT_POL	**INT_POL.** Sets the active polarity for the interrupt status when reflected on the INT_C1B output pin. 0: Active low 1: Active high

Register 23.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						LOS2_ MSK	LOS1_ MSK	LOSX_ MSK
Type	R	R	R	R	R	R/W	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:3	Reserved	
2	LOS2_MSK	**LOS2_MSK.** Determines if a LOS on CKIN2 (LOS2_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS2_FLG register. 0: LOS2 alarm triggers active interrupt on IRQ output (if IRQ=1). 1: LOS2_FLG ignored in generating interrupt output.
1	LOS1_MSK	**LOS1_MSK.** Determines if a LOS on CKIN1 (LOS1_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS1_FLG register. 0: LOS1 alarm triggers active interrupt on IRQ output (if IRQ=1). 1: LOS1_FLG ignored in generating interrupt output.
0	LOSX_MSK	**LOSX_MSK.** Determines if a LOS on OSC (LOSX_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOSX_FLG register. 0: LOSX alarm triggers active interrupt on IRQ output (if IRQ=1). 1: LOSX_FLG ignored in generating interrupt output.

Register 24.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						FOS2_MSK	FOS1_MSK	LOL_MSK
Type	R	R	R	R	R	R/W	R/W	R/W

Reset value = 0011 1111

Bit	Name	Function
7:3	Reserved	
2	FOS2_MSK	**FOS2_MSK.** Determines if the FOS2_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS2_FLG register. 0: FOS2 alarm triggers active interrupt on IRQ output (if IRQ_PIN=1). 1: FOS2_FLG ignored in generating interrupt output.
1	FOS1_MSK	**FOS1_MSK.** Determines if the FOS1_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS1_FLG register. 0: FOS1 alarm triggers active interrupt on IRQ output (if IRQ_PIN=1). 1: FOS1_FLG ignored in generating interrupt output.
0	LOL_MSK	**LOL_MSK.** Determines if the LOL_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the LOL_FLG register. 0: LOL alarm triggers active interrupt on IRQ output (if IRQ_PIN=1). 1: LOL_FLG ignored in generating interrupt output.

Register 25.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1_HS [2:0]							
Type	R/W			R	R	R	R	R

Reset value = 0010 0000

Bit	Name	Function
7:5	N1_HS [2:0]	**N1_HS [2:0].** Sets value for N1 high speed divider which drives NCn_LS (n = 1 to 2) low-speed divider. 000: N1 = 4 001: N1 = 5 010: N1 = 6 011: N1 = 7 100: N1 = 8 101: N1 = 9 110: N1 = 10 111: N1 = 11
4:0	Reserved	

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC1_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC1_LS [19:16]	**NC1_LS [19:16].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2^{20} Valid divider values=[1, 2, 4, 6, ..., 2^{20}]

Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC1_LS [15:8]	**NC1_LS [15:8].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111=2^{20} Valid divider values=[1, 2, 4, 6, ..., 2^{20}]

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC1_LS [19:0]	**NC1_LS [7:0].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111=2^{20} Valid divider values=[1, 2, 4, 6, ..., 2^{20}]

Register 34.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC2_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC2_LS [19:16]	**NC2_LS [19:16].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 0000000000000000000=1 0000000000000000001=2 0000000000000000011=4 0000000000000000101=6 ... 1111111111111111111=2^{20} Valid divider values=[1, 2, 4, 6, ..., 2^{20}]

Register 35.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC2_LS [15:8]	**NC2_LS [15:8].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111=2^{20} Valid divider values=[1, 2, 4, 6, ..., 2^{20}]

Register 36.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC2_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC2_LS [7:0]	**NC2_LS [7:0].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111 = 2^{20} Valid divider values = [1, 2, 4, 6, ..., 2^{20}]

Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_HS [2:0]				N2_LS [19:16]			
Type	R/W			R	R/W			

Reset value = 1100 0000

Bit	Name	Function
7:5	N2_HS [2:0]	**N2_HS [2:0].** Sets value for N2 high speed divider which drives N2LS low-speed divider. 000: 4 001: 5 010: 6 011: 7 100: 8 101: 9 110: 10 111: 11
4	Reserved	
3:0	N2_LS [19:16]	**N2_LS [19:16].** Sets value for N2 low-speed divider, which drives phase detector. 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^{20} Valid divider values = [2, 4, 6, ..., 2^{20}]

Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N2_LS [15:8]	**N2_LS [15:8].** Sets value for N2 low-speed divider, which drives phase detector. 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111 = 2^{20} Valid divider values = [2, 4, 6, ..., 2^{20}]

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [7:0]							
Type	R/W							

Reset value = 1111 1001

Bit	Name	Function
7:0	N2_LS [7:0]	**N2_LS [7:0].** Sets value for N2 low-speed divider, which drives phase detector. 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111 = 2^{20} Valid divider values = [2, 4, 6, ..., 2^{20}]

Register 43.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N31 [18:16]		
Type	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N31 [18:16]	**N31 [18:16].** Sets value for input divider for CKIN1. 000000000000000000 = 1 000000000000000001 = 2 000000000000000010 = 3 ... 111111111111111111 = 2^{19} Valid divider values = [1, 2, 3, ..., 2^{19}]

Register 44.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N31_[15:8]	**N31_[15:8].** Sets value for input divider for CKIN1. 000000000000000000 = 1 000000000000000001 = 2 000000000000000010 = 3 ... 111111111111111111 = 2^{19} Valid divider values = [1, 2, 3, ..., 2^{19}]

Register 45.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N31_[7:0	**N31_[7:0].** Sets value for input divider for CKIN1. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^{19} Valid divider values = [1, 2, 3, ..., 2^{19}]

Register 46.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N32_[18:16]		
Type	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N32_[18:16]	**N32_[18:16].** Sets value for input divider for CKIN1. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^{19} Valid divider values = [1, 2, 3, ..., 2^{19}]

Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N32_[15:8]	**N32_[15:8].** Sets value for input divider for CKIN2. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^{19} Valid divider values = [1, 2, 3, ..., 2^{19}]

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N32_[7:0]	**N32_[7:0].** Sets value for input divider for CKIN2. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^{19} Valid divider values = [1, 2, 3, ..., 2^{19}]

Register 55.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CLKIN2RATE[2:0]			CLKIN1RATE[2:0]		
Type	R	R	R/W			R/W		

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	
5:3	CLKIN2RATE[2:0]	**CLKIN2RATE_[2:0].** CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved
2:0	CLKIN1RATE [2:0]	**CLKIN1RATE[2:0].** CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved

Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							CK2_ACTV_REG	CK1_ACTV_REG
Type	R	R	R	R	R	R	R	R

Reset value = 0010 0000

Bit	Name	Function
7:2	Reserved	
1	CK2_ACTV_REG	**CK2_ACTV_REG.** Indicates if CKIN2 is currently the active clock for the DSPLL input. 0: CKIN2 is not the active input clock. Either it is not selected or LOS2_INT is 1. 1: CKIN2 is the active input clock.
0	CK1_ACTV_REG	**CK1_ACTV_REG.** Indicates if CKIN1 is currently the active clock for the DSPLL input. 0: CKIN1 is not the active input clock. Either it is not selected or LOS1_INT is 1. 1: CKIN1 is the active input clock.

Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						LOS2_INT	LOS1_INT	LOSX_INT
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0110

Bit	Name	Function
7:3	Reserved	
2	LOS2_INT	**LOS2_INT.** Indicates the LOS status on CKIN2. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN2 input.
1	LOS1_INT	**LOS1_INT.** Indicates the LOS status on CKIN1. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN1 input.
0	LOSX_INT	**LOSX_INT.** Indicates the LOS status of the external reference on the OSC pins. 0: Normal operation. 1: Internal loss-of-signal alarm on OSC reference clock input.

Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DIGHOLDVALID				FOS2_INT	FOS1_INT	LOL_INT
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0001

Bit	Name	Function
7	Reserved	
6	DIGHOLDVALID	**Digital Hold Valid.** Indicates if the digital hold circuit has enough samples of a valid clock to meet digital hold specifications. 0: Indicates digital hold history registers have not been filled. The digital hold output frequency may not meet specifications. 1: Indicates digital hold history registers have been filled. The digital hold output frequency is valid.
5:3	Reserved	
2	FOS2_INT	**CKIN2 Frequency Offset Status.** 0: Normal operation. 1: Internal frequency offset alarm on CKIN2 input.
1	FOS1_INT	**CKIN1 Frequency Offset Status.** 0: Normal operation. 1: Internal frequency offset alarm on CKIN1 input.
0	LOL_INT	**PLL Loss of Lock Status.** 0: PLL locked. 1: PLL unlocked.

Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						LOS2_FLG	LOS1_FLG	LOSX_FLG
Type	R	R	R	R	R	R/W	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:3	Reserved	
2	LOS2_FLG	**CKIN2 Loss-of-Signal Flag.** 0: Normal operation. 1: Held version of LOS2_INT. Generates active output interrupt if output interrupt pin is enabled (IRQ_PIN = 1) and if not masked by LOS2_MSK bit. Flag cleared by writing 0 to this bit.
1	LOS1_FLG	**CKIN1 Loss-of-Signal Flag.** 0: Normal operation 1: Held version of LOS1_INT. Generates active output interrupt if output interrupt pin is enabled (IRQ_PIN = 1) and if not masked by LOS1_MSK bit. Flag cleared by writing 0 to this bit.
0	LOSX_FLG	**External Reference (signal on pins XA/XB) Loss-of-Signal Flag.** 0: Normal operation 1: Held version of LOSX_INT. Generates active output interrupt if output interrupt pin is enabled (IRQ_PIN = 1) and if not masked by LOSX_MSK bit. Flag cleared by writing 0 to this bit.

Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					FOS2_FLG	FOS1_FLG	LOL_FLG	
Type	R	R	R	R	R/W	R/W	R/W	R

Reset value = 0000 0010

Bit	Name	Function
7:4	Reserved	
3	FOS2_FLG	**CLKIN_2 Frequency Offset Flag.** 0: Normal operation. 1: Held version of FOS2_INT. Generates active output interrupt if output interrupt pin is enabled (IRQ_PIN = 1) and if not masked by FOS2_MSK bit. Flag cleared by writing 0 to this bit.
2	FOS1_FLG	**CLKIN_1 Frequency Offset Flag.** 0: Normal operation 1: Held version of FOS1_INT. Generates active output interrupt if output interrupt pin is enabled (IRQ_PIN = 1) and if not masked by FOS1_MSK bit. Flag cleared by writing 0 to this bit.
1	LOL_FLG	**PLL Loss of Lock Flag.** 0: PLL locked 1: Held version of LOL_INT. Generates active output interrupt if output interrupt pin is enabled (IRQ_PIN = 1) and if not masked by LOL_MSK bit. Flag cleared by writing 0 to this bit.
0	Reserved	

Register 134.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [11:4]							
Type	R							

Reset value = 0000 0001

Bit	Name	Function
7:0	PARTNUM_RO [11:0]	**Device ID (1 of 2).** 0000 0100 1010: Si5374 Others: Reserved

Register 135.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [3:0]				REVID_RO [3:0]			
Type	R				R			

Reset value = 1010 0010

Bit	Name	Function
7:4	PARTNUM_RO [11:0]	**Device ID (2 of 2).** 0000 0100 1010: Si5374 Others: Reserved
3:0	REVID_RO [3:0]	**Indicates Device Revision Level.** 0010: Revision C Others: Reserved.

Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RST_REG	ICAL						
Type	R/W	R/W	R	R	R	R	R	R

Reset value = 0000 0000

Bit	Name	Function
7	RST_REG	**Internal Reset (Same as Pin Reset).** **Note:** The I^2C port may not be accessed until 10 ms after RST_REG is asserted. 0: Normal operation. 1: Reset all internal logic. Outputs disabled or tristated during reset.
6	ICAL	**Start Internal Calibration Sequence.** For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a one to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. A valid stable clock (within 100 ppm) must be present to begin ICAL. Note: Any divider, CLKINn_RATE or BWSEL_REG changes require an ICAL to take effect. 0: Normal operation. 1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-calibration, LOL will go low.
5:0	Reserved	

Register 137.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								FASTLOCK
Type	R	R	R	R	R	R	R	R/W

Reset value = 0000 0000

Bit	Name	Function
7:1	Reserved	Do not modify.
0	FASTLOCK	**This bit must be set to 1 to enable FASTLOCK.** This improves initial lock time by dynamically changing the loop bandwidth during PLL lock acquisition.

Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOS2_EN [1:1]	LOS1_EN [1:1]
Type	R	R	R	R	R	R	R/W	R/W

Reset value = 0000 1111

Bit	Name	Function
7:2	Reserved	
1	LOS2_EN [1:0] MSB	**Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).** **Note:** LOS2_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.
0	LOS1_EN [1:0] MSB	**Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.

Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			LOS2_EN [0:0]	LOS1_EN [0:0]			FOS2_EN	FOS1_EN
Type	R	R	R/W	R/W	R	R	R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7:6	Reserved	
5	LOS2_EN [1:0] LSB	**Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).** Note: LOS2_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.
4	LOS_EN [1:0] LSB	**Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.
3:2	Reserved	
1	FOS2_EN	**Enables FOS on a Per Channel Basis.** 0: Disable FOS monitoring. 1: Enable FOS monitoring.
0	FOS1_EN	**Enables FOS on a Per Channel Basis.** 0: Disable FOS monitoring. 1: Enable FOS monitoring.

Register 142.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW1 [7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPENDENTSKEW1 [7:0]	**INDEPENDENTSKEW1.** Eight-bit field that represents a 2s complement of the phase offset in terms of clocks from the high speed output divider. Default = 0.

Register 143.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW2 [7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPENDENTSKEW2 [7:0]	**INDEPENDENTSKEW2.** 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. Default = 0.

7.1. ICAL

The device registers must be configured for the device operation. After device configuration, a calibration procedure must be performed once a stable clock is applied to the selected CKINn input. The calibration process is triggered by writing a “1” to bit D6 in register 136. See the Family Reference Manual for details. In addition, after a successful calibration operation, changing any of the registers indicated in Table 9 requires that a calibration be performed again by the same procedure (writing a “1” to bit D6 in register 136).

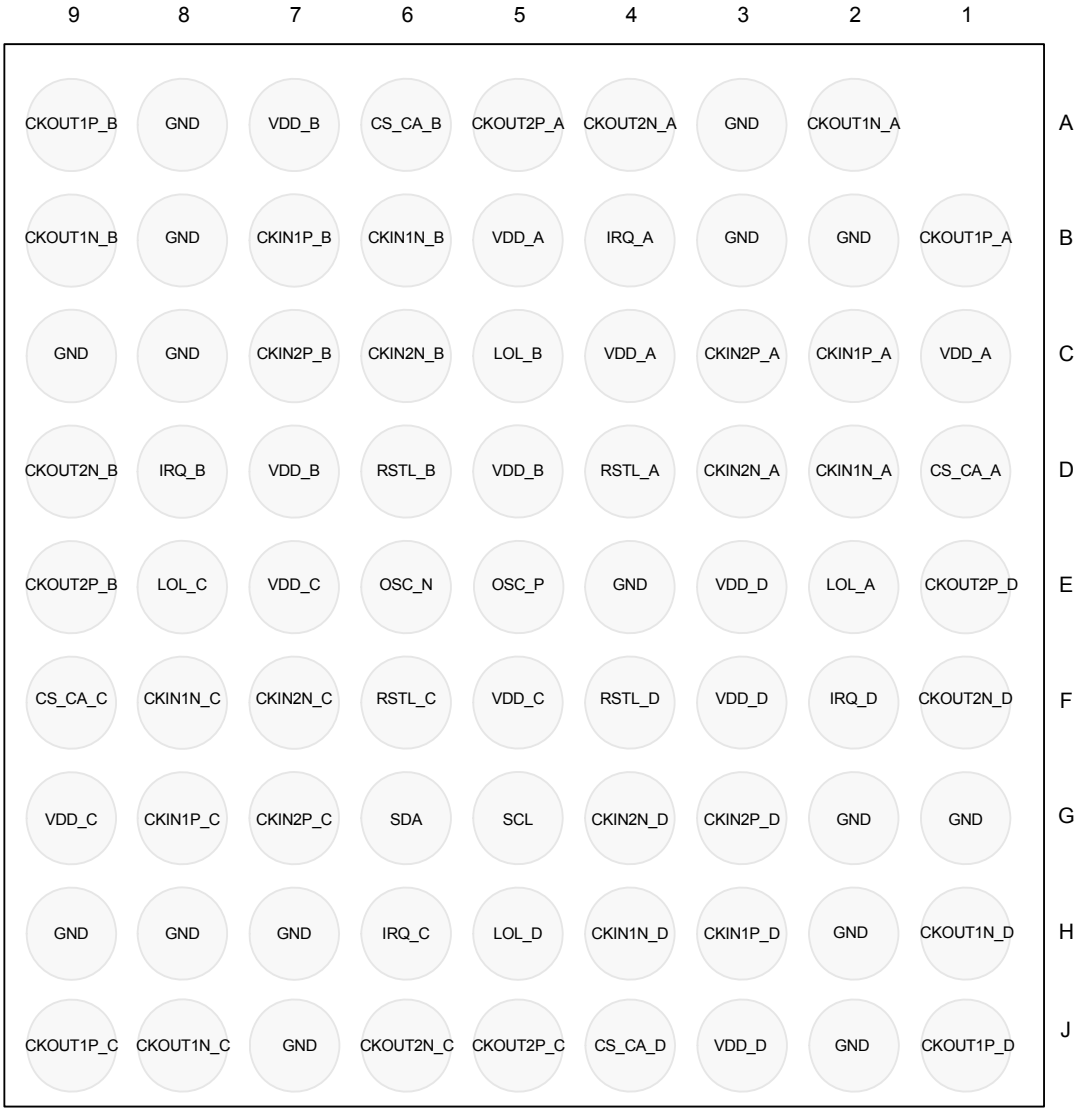
Table 9. ICAL-Sensitive Registers

Address	Register
0	BYPASS_REG
0	CKOUT_ALWAYS_ON
1	CK_PRIOR1
1	CK_PRIOR2
2	BSWEL_REG
2	RATE_REG
4	HIST_DEL
5	ICMOS
7	FOSREFSEL
9	HIST_AVG
10	DSBL1_REG
10	DSBL2_REG
11	PD_CK1
11	PD_CK2
19	FOS_EN
19	FOS_THR
19	LOCKT
19	VALTIME
25	N1_HS
31	NC1_LS
34	NC2_LS
40	N2_HS
40	N2_LS
43	N31
46	N32
55	CLKIN1RATE
55	CLKIN2RATE

Table 10. CKOUT_ALWAYS_ON and SQ_ICAL Truth Table

CKOUT_ALWAYS_ON	SQ_ICAL	Results
0	0	CKOUT OFF until after the first ICAL
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low)
1	0	CKOUT always ON, including during an ICAL
1	1	CKOUT always ON, including during an ICAL. Use these settings to preserve output-to-output skew

8. Pin Descriptions: Si5374


9 8 7 6 5 4 3 2 1
CKOUT1P_B GND VDD_B CS_CA_B CKOUT2P_A CKOUT2N_A GND CKOUT1N_A A
CKOUT1N_B GND CKIN1P_B CKIN1N_B VDD_A IRQ_A GND GND CKOUT1P_A B
GND GND CKIN2P_B CKIN2N_B LOL_B VDD_A CKIN2P_A CKIN1P_A VDD_A C
CKOUT2N_B IRQ_B VDD_B RSTL_B VDD_B RSTL_A CKIN2N_A CKIN1N_A CS_CA_A D
CKOUT2P_B LOL_C VDD_C OSC_N OSC_P GND VDD_D LOL_A CKOUT2P_D E
CS_CA_C CKIN1N_C CKIN2N_C RSTL_C VDD_C RSTL_D VDD_D IRQ_D CKOUT2N_D F
VDD_C CKIN1P_C CKIN2P_C SDA SCL CKIN2N_D CKIN2P_D GND GND G
GND GND GND IRQ_C LOL_D CKIN1N_D CKIN1P_D GND CKOUT1N_D H
CKOUT1P_C CKOUT1N_C GND CKOUT2N_C CKOUT2P_C CS_CA_D VDD_D GND CKOUT1P_D J

Bottom View

Figure 9. Si5374 Pin Configuration (Bottom View)

Table 11. Si5374 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
D4 D6 F6 F4	RSTL_A RSTL_B RSTL_C RSTL_D	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of all four DSPLLs. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tri-stated during reset. The part must be programmed after a reset or power-on to get a clock output. This pin has a weak pull-up.
B4 D8 H6 F2	IRQ_A IRQ_B IRQ_C IRQ_D	O	LVCMOS	**DSPLLq Interrupt Indicator.** This pin functions as a device interrupt output. The interrupt output, *IRQ_PINn* must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the *IRQ_POLn* register bit. 0 = CKINn present 1 = LOS (FOS) on CKINn The active polarity is controlled by *CK_BAD_POL*. If no function is selected, the pin tri-states.
C1, C4, B5 A7, D5, D7 E7, F5, G9 E3, F3, J3	VDD_A VDD_B VDD_C VDD_D	V_{DD}	Supply	**Supply.** The device operates from a 1.8 or 2.5 V supply. A 0.1 µF bypass capacitive is required for every VDD_9 pin. Bypass capacitors should be associated with the following VDD_q pins: 0.1 µF per VDD pin. Four 1.0 µF should also be placed as close to each VDD domain as is practical. See recommended layout.
E5 E6	OSC_P OSC_N	I	Analog	**External OSC.** An external low jitter reference clock should be connected to these pins. See the any-frequency precision clocks family reference manual for oscillator selection details.
Note: Internal register names are indicated by italics, e.g., *IRQ_PIN*. See Si5374 Register Map.				

Table 11. Si5374 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
B2 A3 B3 E4 C8 A8 B8 C9 H7 J7 H8 H9 G1 H2 J2 G2	GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND	GND	Supply	**Ground for each DSPLLq.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device. See recommended layout.
C2 D2 C3 D3 B7 B6 C7 C6 G8 F8 G7 F7 H3 H4 G3 G4	CKIN1P_A CKIN1N_A CKIN2P_A CKIN2N_A CKIN1P_B CKIN1N_B CKIN2P_B CKIN2N_B CKIN1P_C CKIN1N_C CKIN2P_C CKIN2N_C CKIN1P_D CKIN1N_D CKIN2P_D CKIN2N_D	I	Multi	**Clock Inputs for DSPLLq.** Differential input clocks. This input can also be driven with a single-ended signal.
Note: Internal register names are indicated by italics, e.g., *IRQ_PIN*. See Si5374 Register Map.				

Table 11. Si5374 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
E2 C5 E8 H5	LOL_A LOL_B LOL_C LOL_D	O	LVCMOS	**DSPLLq Loss of Lock Indicator.** These pins function as the active high PLL loss of lock indicator if the *LOL_PIN* register bit is set to 1. 0 = PLL locked. 1 = PLL unlocked. If *LOL_PINn* = 0, this pin will tri-state. Active polarity is controlled by the *LOL_POLn* bit. The PLL lock status will always be reflected in the *LOL_INTn* read only register bit (see application note, "AN803: Lock and Settling Time Considerations for the Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs).
D1 A6 F9 J4	CS_CA_A CS_CA_B CS_CA_C CS_CA_D	I/O	LVCMOS	**DSPLLq Input Clock Select/Active Clock Indicator.** **Input**: In manual clock selection mode, this pin functions as the manual input clock selector if the *CKSEL_PIN* is set to 1. 0 = Select CKIN1 1 = Select CKIN2 If *CKSEL_PIN* = 0, the *CKSEL_REG* register bit controls this function and this input tristates. If configured for input, must be tied high or low. **Output**: In automatic clock selection mode, this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both clocks, CK_ACTV will indicate the last active clock that was used before entering the digital hold state. The *CK_ACTV_PIN* register bit must be set to 1 to reflect the active clock status to the CK_ACTV output pin. 0 = CKIN1 active input clock 1 = CKIN2 active input clock If *CK_ACTV_PIN* = 0, this pin will tristate. The CK_ACTV status will always be reflected in the *CK_ACTV_REG* read only register bit.
G5	SCL	I	LVCMOS	**I^2C Serial Clock.** This pin functions as the serial clock input. This pin has a weak pull-down.
G6	SDA	I/O	LVCMOS	**I^2C Serial Data.** I^2C pin functions as the bi-directional serial data port.
Note: Internal register names are indicated by italics, e.g., *IRQ_PIN*. See Si5374 Register Map.				

Table 11. Si5374 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
B1 A2 A5 A4 A9 B9 E9 D9 J9 J8 J5 J6 J1 H1 E1 F1	CKOUT1P_A CKOUT1N_A CKOUT2P_A CKOUT2N_A CKOUT1P_B CKOUT1N_B CKOUT2P_B CKOUT2N_B CKOUT1P_C CKOUT1N_C CKOUT2P_C CKOUT2N_C CKOUT1P_D CKOUT1N_D CKOUT2P_D CKOUT2N_D	O	Multi	**Output Clock for DSPLLq.** Differential output clocks. Output signal format is selected by *SFOUT_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive in phase single-ended clock outputs at the same frequency.
Note: Internal register names are indicated by italics, e.g., *IRQ_PIN*. See Si5374 Register Map.				

9. Ordering Guide

Ordering Part Number	Input/Output Clocks	PLL Bandwidth Range	Package	RoHS6 Pb-Free	Temperature Range
Si5374B-A-GL[1]	8/8	4 to 525 Hz	10x10 mm 80-PBGA	Yes	–40 to 85 °C
Si5374B-A-BL[1]	8/8	4 to 525 Hz	10x10 mm 80-PBGA	No	–40 to 85 °C
Si5374C-A-GL[2]	8/8	4 to 525 Hz	10x10 mm 80-PBGA	Yes	–40 to 85 °C
Si5374C-A-BL[2]	8/8	4 to 525 Hz	10x10 mm 80-PBGA	No	–40 to 85 °C
Si5374-EVB			Evaluation Board		

Notes:

1. These two OPNs are recommended for all new designs. Refer to application note, “AN803: Lock and Settling Time Considerations for Si5324/27/69/74 Any Frequency Jitter Attenuating Clock ICs” for more information.
2. These two OPNs are intended for use in legacy designs in which the Si5374 device must retain the original lock time behavior as described in AN803 and Product Bulletin (PB-1312191): “Si5324, Si5327, Si5369, Si5374 Loss-of-Lock (LOL) Time Behavior: New Applications Note and Ordering Options”.

10. Package Outline

Figure 10 illustrates the package details for the Si5374. Table 12 lists the values for the dimensions shown in the illustration.

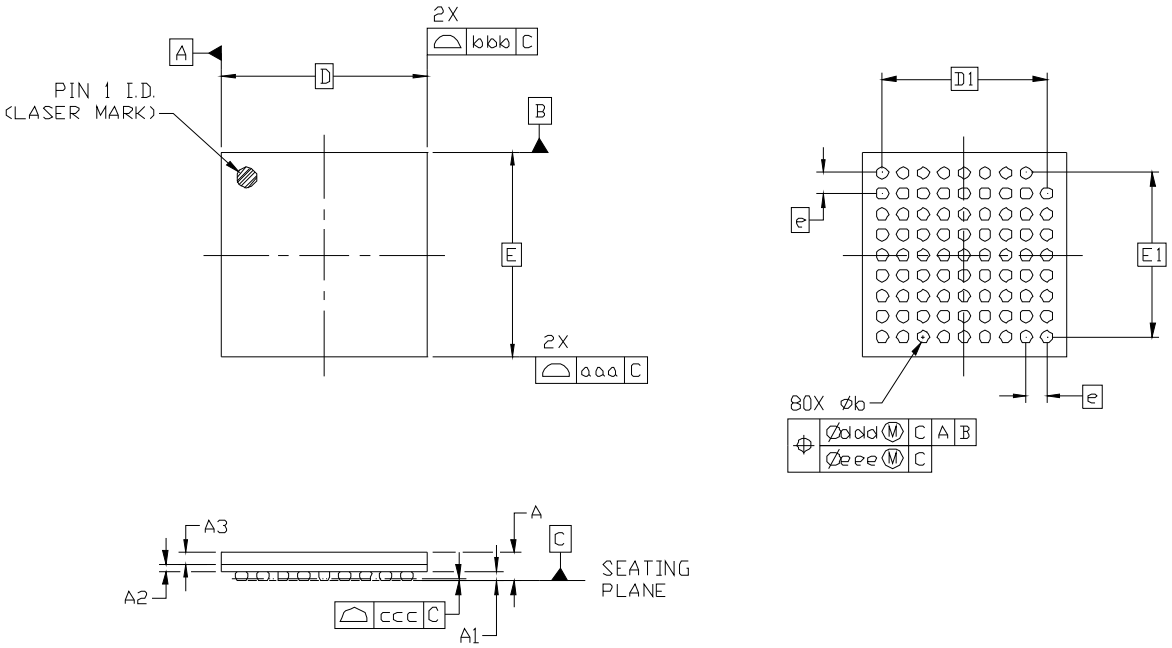


Figure 10. 80-Pin Plastic Ball Grid Array (PBGA)

Table 12. Package Dimensions

Symbol	Min	Nom	Max
A	1.22	1.39	1.56
A1	0.40	0.50	0.60
A2	0.32	0.36	0.40
A3	0.46	0.53	0.60
b	0.50	0.60	0.70
D	10.00 BSC		
E	10.00 BSC		
D1	8.00 BSC		

	Min	Nom	Max
E1	8.00 BSC		
e	1.00 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.12		
ddd	0.15		
eee	0.08		

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-192.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Recommended PCB Layout

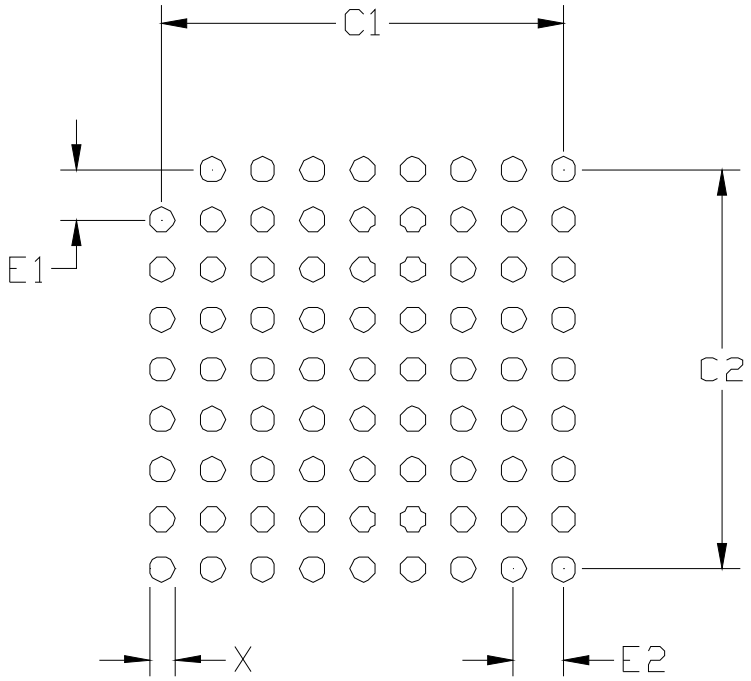


Figure 11. PBGA Card Layout

Table 13. Layout Dimensions

Symbol	MIN	NOM	MAX
X	0.40	0.45	0.50
C1		8.00	
C2		8.00	
E1		1.00	
E2		1.00	

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Markings

12.1. Si5374 Top Marking (PBGA, Lead-Free)

12.2. Top Marking Explanation (PBGA, Lead-Free)

Mark Method:	Laser	
Logo Size:	6.1 x 2.2 mm Center-Justified	
Font Size:	0.80 mm Right-Justified	
Line 1 Marking:	Device Part Number	Si5374B-A-GL, Pb-free
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	“e1” Lead-Free Finish Symbol (Pb-Free BGA Balls)	Circle = 1.4 mm Diameter Center-Justified
	Country of Origin	TW

12.3. Si5374 Top Marking (PBGA, Lead-Finish)

12.4. Top Marking Explanation (PBGA, Lead-Finish)

Mark Method:	Laser	
Logo Size:	6.1 x 2.2 mm Center-Justified	
Font Size:	0.80 mm Right-Justified	
Line 1 Marking:	Device Part Number	Si5374B-A-BL, Pb finish
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	“e0” Lead Finish Symbol (SnPb BGA Balls)	Circle = 1.4 mm Diameter Center-Justified
	Country of Origin	TW

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Added 1.8 V operation.
- Added 40 MHz reference oscillator
- Corrected Figure 10 title.
- Added comment to SFOUT register.

Revision 0.2 to Revision 0.3

- Updated and reordered spec tables.

Revision 0.3 to Revision 0.4

- Added Silicon Labs logo to device top mark.

Revision 0.4 to Revision 0.45

- Added comments indicating that a crystal may not be used in place of an external oscillator.
- Updated specification Tables 3, 4, and 5.
- Added maximum jitter specifications to Table 5.
- Added Thermal Characteristics table on page 12.
- Added Figure 3, “Typical Phase Noise Plot,” on page 14.
- Added "5. Si5374 Application Examples and Suggestions" on page 17.
- Updated "7. Register Descriptions" on page 22.
- Added a part number for the non-RoHS6 device to "9. Ordering Guide" on page 63.
- Added recommendations on the four reset pins in "5.4. RSTL_x Pins" on page 17.
- Added Lead-Finish top marking.

Revision 0.45 to Revision 1.0

- Updated " Features" on page 1.
  - Revised output jitter values.
- Minor corrections to Tables 2 and 3.
- Added maximum lock and settle time specs to Table 5.
- Updated "5.5. Reference Oscillator Selection" on page 17.
  - Revised Si530 part number.
- Added warning about MEMS reference oscillators to "5.5. Reference Oscillator Selection" on page 17.
- Added Table 10 in "7.1. ICAL" on page 56.

Revision 1.0 to Revision 1.1

- Added reference to AN803 on pages 11, 16, 31 and 60.
- Added additional LOL and Settling Time Specs on page 11.
- Added new part numbers on page 63.
- Updates to LOS1_EN and LOS2_EN on pages 53 and 54.

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and register to submit a technical support request.

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